

ABSTRACT OF DISCLOSURE

An error correction coding apparatus includes a parity check matrix generation unit which generates a parity check matrix having a number of elements having a value of 1 in each row thereof, having a predetermined number of elements having a value of 1 in each column thereof, and having the other elements having a value of 0; a parity check matrix adjustment unit which receives the parity check matrix from the parity check matrix generation unit, searches the parity check matrix for a cycle forming group of four elements positioned at respective vertexes of a rectangle and having a value of 1, and when there is at least one cycle forming group, replaces the value of 1 of at least one element of the cycle forming group with the value 0 of another element, to output an adjusted parity check matrix without a cycle forming group therein; and an LDPC coding unit which receives the adjusted parity check matrix from the parity check matrix adjustment unit and receives an m-bit message word to perform LDPC coding.